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09/026,790	02/20/1998	GUY DUPENLOUP	30454-122(P-	2246

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EXAMINER	
THOMPSON, ANNETTE M	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/026,790	Applicant(s) DUPENLOUP, GUY	
	Examiner A. M. Thompson	Art Unit 2825	

-- Th MAILING DATE of this communication appears on the cover sh et with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

With the authorization of the 2800 Technology Center Director, PROSECUTION IS HEREBY REOPENED in this case. A new ground of rejection is set forth below. Claims 1-6, 9-20 are pending.

Claim Objections

1. Claims 1-6, 9-20 are objected to for the following reasons: Pursuant to claim 1, at line 6, "Generic" should be lower case, i.e. - -generic--; additionally, at line 2 before "gate" insert - -a- -. Pursuant to claims 1, 2, 3 and 6, "the IC design" lacks sufficient antecedent basis. Pursuant to claims 9 and 14 (line 8), claims 10, 11, 13 (line 7), "the IC design" lacks antecedent basis; the preamble references a plurality of IC designs and therefore does not provide antecedent basis for a singular IC design. Correction involves either changing "the" to - -an- - or using the plural of "design".

2. Pursuant to claim 5, at line 2, "the design" lacks sufficient antecedent basis; furthermore is is unclear whether "the design" references IC design or design structure.

3. Pursuant to claims 9, 10, 11, 13, and 14, at the last line before "the IC design", change "and" to - -of- -

4. Pursuant to claim 11, at line 4, before "generic" replace the article "the" with - -a- - to provide correct antecedent basis.

5. Pursuant to claim 12, at line 1, change "A" to - -The- -.

6. Pursuant to claim 13, at line 4, "the generic netlist" lacks sufficient antecedent basis.

7. Pursuant to claims 9, 10, 11, 13, and 14, all instances of "description" should be plural.

8. Pursuant to claim 2-6, at line 1, before "method", change "A" to "The". Pursuant to claim 12 and claims 15-20, before "computer", change "A" to --The- -.

9. Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1-6, 9-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claims 1, 9-11, 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Pursuant to claims 1, 9-11, 13 and 14, the omitted structural cooperative relationships are between "constraints", the logic synthesis tool, and the IC design.

13. Claims 1, 9, 11, 13, 14, 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Pursuant to claims 1, 9, 11, 13, 14, 15-20, the omitted structural cooperative relationships are between the top down characterization and the capturing of the I/O conditions and constraints of the modules of the IC design. The dependent claims 15-20 recite "wherein I/O conditions and

constraints of the modules of the IC design captured during the top-down characterization." However, the independent claims from which these claims depend do not recite a limitation wherein I/O conditions and constraints are captured during any process.

14. Claims 9, 10, 11, 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Pursuant to claims 9, 10, 11, 13, and 14, the omitted functional/structural cooperative relationships are between the "generic netlist", the "RTL description", the "gate-level" description, and the IC design. The relationship between the IC design and the generic netlist is unclear, i.e. what does determining key pins in a generic netlist and extracting critical design structure and hierarchy from a generic netlist have to do with bottom-up synthesis and top-down characterization of an IC design and how does this all relate to the RTL level description and gate level description.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of claims 1-6 and 9-20

16. **Claims 1-6 and 9-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupte et al. (Gupte), U.S. Patent 5,812,416 in view of Hemmi et al. (Hemmi), U.S. Patent 5,615,124 and Beausang et al. (Beausang), U.S. Patent 5,903,466. Gupte discloses methods and systems for generating synthesis scripts for integrated circuit designs. In disclosing the method of generating synthesis scripts to synthesize integrated circuit designs from a generic netlist description, Gupte inputs HDL code. Gupte does not explicitly disclose the use of a generic netlist or the term generic netlist. However, Hemmi at column 1, lines 21-31 teaches that HDL, a common acronym in the art for hardware description language, represents an integrated circuit netlist. Although Hemmi teaches that the HDL code (Hemmi uses the term description instead of code) is a netlist, Hemmi does not explicitly disclose the meaning of the term *generic* netlist. Beausang discloses that a generic netlist means that a netlist is technology independent (column 1, line 61 to col. 2, line 4) and further that being technology independent means that the netlist has not yet been correlated with a technology library. Gupte teaches HDL code that has not been correlated with a technology library. Therefore, Gupte's HDL code is synonymous with a generic netlist. It would have been obvious to one of ordinary skill in the art to reference and use the teachings of Hemmi and Beausang for a clear understanding of what HDL code and generic netlist represents and to use the teachings of these references in combination with Gupte to define what Gupte at least suggests if not teaches, i.e. that to one of ordinary skill in the art, Gupte's HDL code corresponds to a generic netlist. See also Ginetti, U.S. Patent 5,396,435, col. 1, ll. 19-30, which discloses the meaning of the term netlist.

17. Pursuant to claim 1, which recites [a] method of generating synthesis scripts to synthesize integrated circuit designs from a generic netlist description into a gate-level description (col. 3, ll. 8-10, ll. 22-34; see also claim 1), said method comprising the steps of : identifying hardware elements in the generic netlist (col. 14, ll. 12-17);

determining key pins for each of said identified hardware elements (col. 9, ll. 58-64);

extracting design structure and hierarchy from the generic netlist (col. 14, ll. 12-22);

generating script to cause a logic synthesis tool to apply bottom-up synthesis to modules and sub-modules of the IC design (col. 14, ll. 32-35, ll. 39-48);

generating script to cause a logic synthesis too to apply top-down characterization to modules and sub-modules of the IC design (col. 14, ll. 49-52); and

generating script to cause a logic synthesis tool to repeat said bottom-up and said top-down applications until constraints are satisfied (see Figure 14 which illustrates the top-down and bottom-up synthesization process, and especially step 812 which emphasizes that these processes are repeated. Also see col. 14, ll. 52-55).

18. Pursuant to claim 2, wherein the step of extracting design structure allows for a multilevel structuring of modules of the IC design (col. 14, line 65 to col. 16, line 24, wherein various commands are used to impact a designs hierarchy).

19. Pursuant to claim 3, further comprising the step of generating script to cause a logic synthesis tool to apply initial mapping to the IC design (Figure 12; col. 13, ll. 10-49; Figure 14, step 800; col. 14, ll. 39-41).

20. Pursuant to claim 4, wherein the logic synthesis tool is a Synopsys Design Compiler (col. 7, ll. 6-19, wherein an embodiment of the Gupte invention uses the Synopsys Design compiler.

21. Pursuant to claim 5, further comprising the step of rearranging design hierarchy by changing the design (col. 3, ll. 8-21, wherein Gupte teaches that incremental changes to design modules may result in hierarchical changes.

22. Pursuant to claim 6, further comprising the step of generating script to cause a logic synthesis tool to ungroup modules of the IC design (Figs. 15B and 15C; col. 14, ll. 65-67; col. 15, ll. 43-67; col. 16, ll. 1-24, wherein Gupte teaches a method in which a recipe file that performs an UNGROUP procedure is processed during script generation.

23. Pursuant to claim 9, which recites [a]n apparatus for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description (col. 5, line 58 to col. 6, line 28), comprising: a processor (Fig. 2, block 102; col. 6, ll. 9-17); memory connected to said processor (Fig. 2, block 104; col. 6, ll. 9-17); said memory having instructions for said processor (col. 5, ll. 58-67) to determine key pins for identified hardware elements from a generic netlist (col. 9, ll. 58-64); extract critical design structure and hierarchy from the generic netlist (col. 14, ll. 12-22); apply bottom-up synthesis to modules and sub-modules of the IC design (col. 14, ll. 32-35, ll. 39-48); apply top-down characterization to modules and sub-modules of the IC design (col. 14, ll. 49-52); repeat said bottom-up and said top-down applications until constraints are satisfied (Fig. 14, step 812 which illustrates top-down and bottom-up synthesization processes; col. 14, ll. 52-55); and create design compile scripts to synthesize modules and sub-modules of the IC design having said satisfied constraints (col. 14, ll. 39-55).

24. Pursuant to claim 10, which recites which recites [a]n apparatus for generating synthesis scripts to synthesize integrated circuit designs in RTL level description into

gate-level description (Fig. 1, 2; col. 5, line 58 to column 6, line 28), comprising means for determining key pins for identified hardware elements from a generic netlist (Figure 5, step 350; col. 8, ll. 43-64, wherein the inputs/outputs listed are key pins; Fig. 6, steps 406, 408; col. 9, ll. 47-65); means for extracting critical design structure and hierarchy from the generic netlist (col. 14, ll. 12-22); means for applying bottom-up synthesis to modules and sub-modules of an IC design (col. 14, ll. 32-35, ll. 39-48); means for applying top-down characterization to modules and sub-modules of the IC design (col. 14, ll. 49-52); means for repeating said bottom-up and said top-down applications until constraints are satisfied (col. 14, ll. 52-55; Figure 14 illustrates the bottom-up and top-down synthesization process); and means for creating design compile scripts to synthesize modules and sub-modules of the IC design having said satisfied constraints (col. 14, ll. 39-55).

25. Pursuant to claim 11 which recites a computer storage medium containing instructions for generating synthesis scripts to synthesize integrated circuit designs in RTL description into gate-level description (Figure 1, col. 5, line 58 to col. 6, line 5), said instructions comprising the steps of identifying hardware elements in a generic netlist (col. 14, ll. 12-17); determining key pins for each of said identified hardware elements (Fig. 5, step 350; col. 8, ll. 43-64 wherein the inputs/outputs listed are key pins; Fig. 6, steps 406, 408; col. 9, ll. 47-65); extracting critical design structure and hierarchy from the generic netlist (col. 14, ll. 12-22); applying bottom-up synthesis to modules and sub-modules of the IC design (col. 14, ll. 32-35, ll. 39-48); applying top-down characterization to modules and sub-modules of the IC design (col. 14, ll. 49-52); repeating said bottom-up and said top-down applications until constraints are satisfied

(Fig. 14, step 812, col. 14, ll. 52-55); and creating design compile scripts to synthesize modules and sub-modules of the IC design having satisfied constraints (col. 14, ll. 39-55).

26. Pursuant to claim 12, wherein said computer storage medium is selected from a group consisting of magnetic device, optical device, magneto-optical device, floppy diskette, CD-ROM, magnetic tape, computer hard drive, and memory card (col. 5, line 63 to col. 6, line 2, wherein Gupte teaches the use of other computer-readable media in addition to a floppy disk).

27. Pursuant to claim 13, which recites [a] process for generating synthesis scripts to synthesize integrated circuits in RTL description into gate-level description (Figs. 13, 14; col. 14, ll. 4-48), said process comprising identifying hardware elements in a generic netlist (col. 14, ll. 12-17); determining key pins for each of said identified hardware elements (Fig. 5, step 350; col. 8, ll. 43-64; Fig. 6, steps 406, 408; col. 9, ll. 47-65); extracting critical design structure and hierarchy from the generic netlist (col. 14, ll. 12-22); applying bottom-up synthesis to modules and sub-modules of the IC design (col. 14, ll. 32-35; ll. 39-48); applying top-down characterization to modules and sub-modules of the IC design (col. 14, ll. 49-53); repeating said bottom-up and said top-down applications until constraints are satisfied (Fig. 14,step 812 illustrates the bottom-up and top-down synthesization process; col. 14, ll. 52-55); and creating design compile scripts to synthesize modules and sub-modules of the IC design having said satisfied constraints (col. 14, ll. 39-55).

28. Pursuant to claim 14, which recites [a] computer system for generating synthesis scripts to synthesize IC design in RTL level descriptions into gate level descriptions (col.

13, ll. 10-67 to col. 14, ll. 1-3), said system comprising means for determining key pins for identified hardware elements from a generic netlist (Fig. 5, step 350; col. 8, ll. 43-64; Fig. 6, steps 406, 408; col. 9, ll. 47-65); means for extracting critical design structure and hierarchy from the generic netlist (col. 14, ll. 12-22); means for applying bottom-up synthesis to modules and sub-modules of the IC design (col. 14, ll. 32-35; ll. 39-48); means for applying top-down characterization to modules and sub-modules of the IC design (col. 14, ll. 49-52); means for repeating said bottom-up and said top-down applications until constraints are satisfied (Fig. 14, step 812; col. 14, ll. 52-55); and means for creating design compile scripts to synthesize modules and sub-modules of the IC design having said satisfied constraints (col. 14, ll. 39-55).

29. Pursuant to claims 15-20, wherein I/O conditions and constraints of the modules of the IC design capture during the top-down characterization are used to re-optimize the IC design during the bottom-up synthesis (col. 14, ll. 12-55).

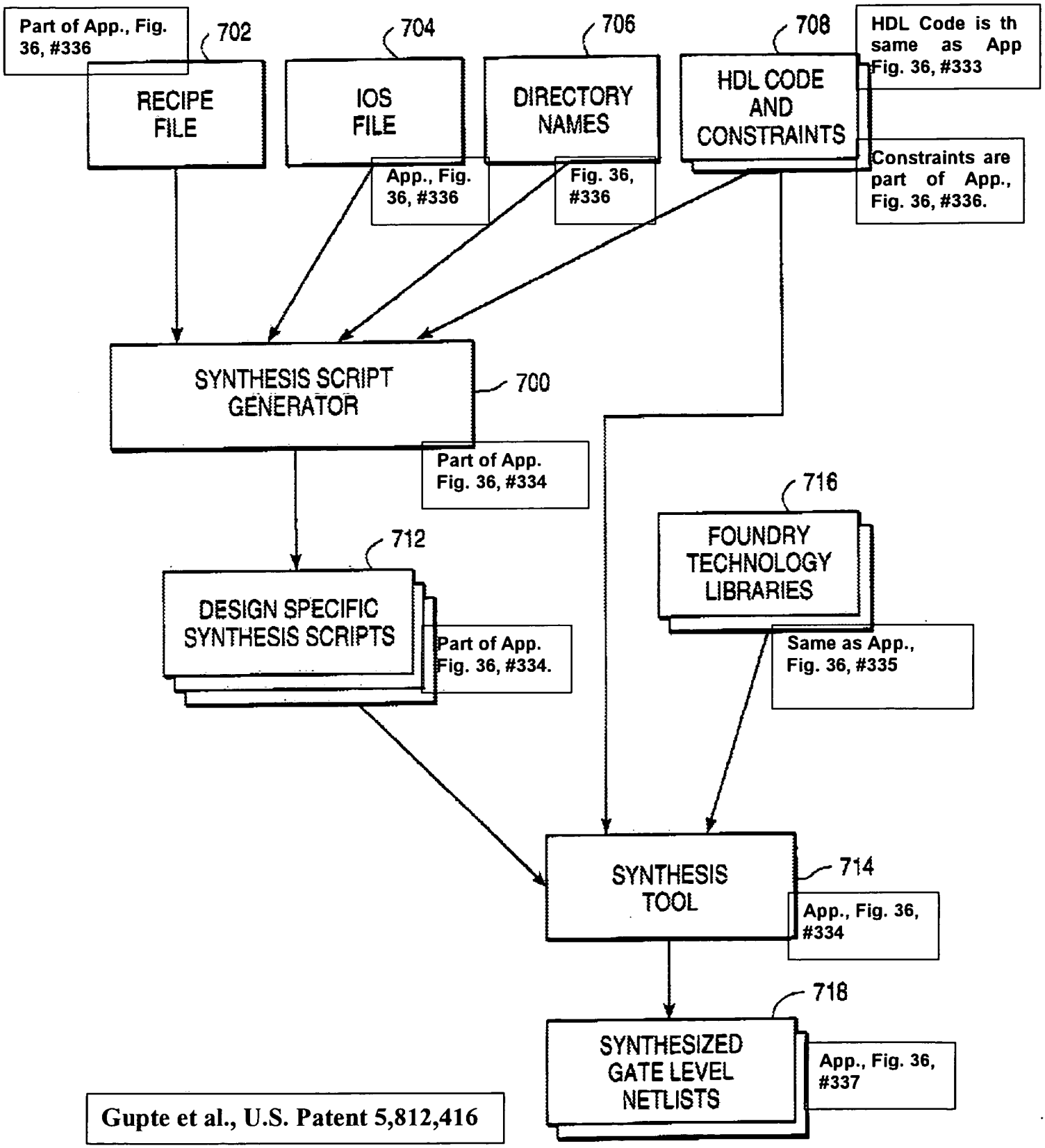
Remarks

Gupte teaches a generic netlist in addition to Applicant's other claimed limitations. Therefore, Applicant's claims are not patentably distinct and are unpatentable over the prior art of record. However, claiming the *creation* of a generic netlist would possibly distinguish Applicant's claims from Gupte.

When the generic netlist of Applicants Figure 36, #333 and Gupte's Fig. 12, #708 has not been correlated with a specific technology library, it is considered general or generic; it not specifically applicable to any particular technology library. The HDL code/generic netlist of Applicant's Fig. 36 and Gupte's Fig. 12 is eventually mapped to a technology specific library. Applicant's Figure 36, #335 illustrates the input of a

technology library along with a generic netlist #333 to a synthesis tool Figure 36, #334 to produce a netlist that is technology specific, Figure 36, #337. This correlates to Gupte's Figure 12, #716, Foundry Technology Libraries, being input along with the Figure 12, #708 HDL code (netlist) to a synthesis tool (Figure 12, #714) to produce a netlist that is technology specific, Figure 12, #716.

The following one-to-one correlation between Applicant's (App.) Figure 36 and Gupte's Figure 12 is depicted below: Applicant's Figure 36, # 333 "Generic Netlist" corresponds to the Gupte Figure 12, #708 "HDL code". Applicant's Figure 36, #336 "User's Design Rules and Constraints" corresponds to the Gupte's Figure 12, #708 "Constraints" together with the additional constraints/rules of Gupte Figure 12, #702, Recipe File, #704, IOS File, and #706, Directory Names. Applicant's Figure 36, #334 "optimization and Mapping" equates to Gupte's Fig. 12 #700, #712, and #714 (The Synthesis Operations). Applicants' Figure 36, #335 "Technology Library" equates to Gupte's Fig. 12, #716 "Foundry Technology Libraries". Applicant's Figure 36, #337 "Technology Netlist, Synthesis Reports" equates to Gupte's Fig. 12, #718 "Synthesized Gate Level Netlists".

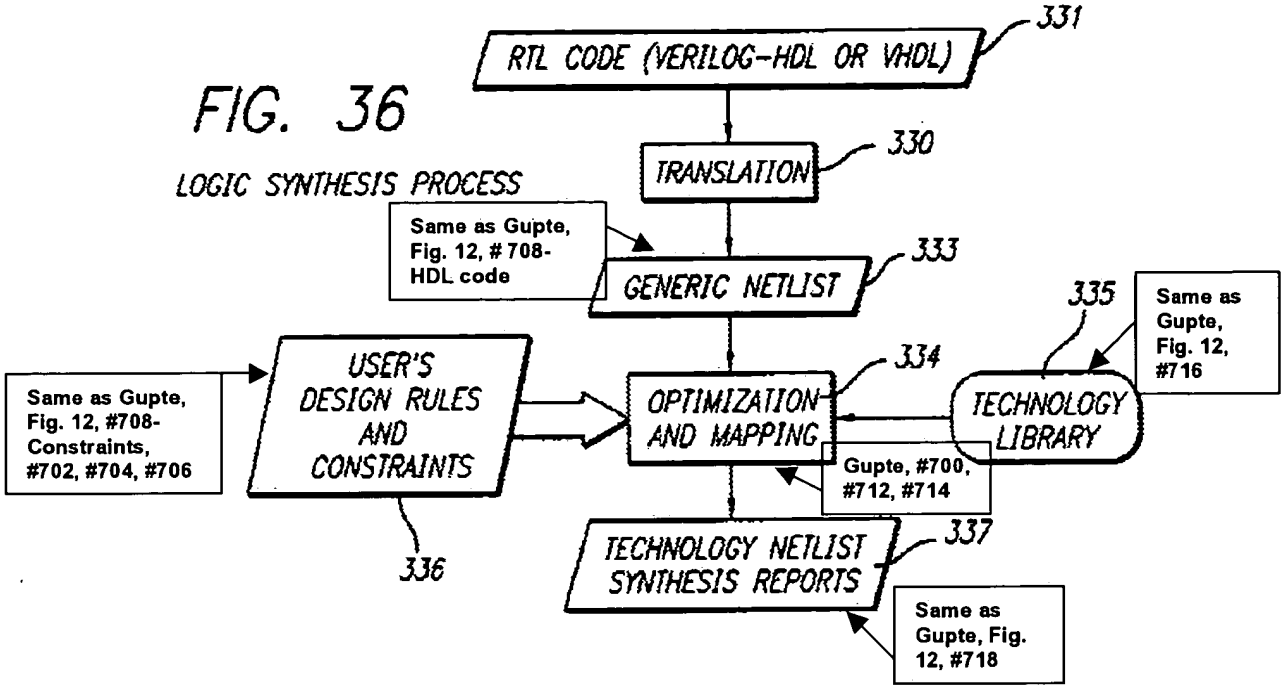


Gupte et al., U.S. Patent 5,812,416

FIG. 12

FIG. 36

LOGIC SYNTHESIS PROCESS



Applicant's Figure 36

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please reference the PTO-892 for a complete listing.

31. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703) 306-3329.

32. Responses to this action should be mailed to:

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